# A 10.6 pJ·K$^2$ Resolution FoM Temperature Sensor Using Astable Multivibrator

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***Abstract*—This brief presents a 0.9-$\mu$W duty-cycle-modulated temperature sensor with a sub-$\mu$A peak current for energy harvester- or micro-battery-powered systems. A compact sensing frontend is proposed to achieve low power, together with various device-level leakage and nonlinearity compensation techniques adopted to minimize the sensor error. In addition, a current-starved multivibrator which provides inherent clamping voltages is used for duty cycle modulation for overall energy savings. The sensor designed in 0.18-$\mu$m CMOS process achieves a resolution figure of merit of 10.6 pJ·K$^2$, which is among the most energy-efficient designs to date. Trimmed at 30 °C, the sensor achieves ±0.85 °C precision from −30 °C to 120 °C. The maximum supply sensitivity is 0.7 °C/V for a 1.6–2 V supply.**

***Index Terms*—CMOS temperature sensor, peak current, self-regulated BGR, bipolar, emitter-coupled astable multivibrator.**

## I. Introduction

THE LAST decade has witnessed a surge in self-powered sensing systems enabled by the development of energy harvesting techniques. Some of these systems are powered by the instantaneous harvested power, e.g., from RF [1], [2], optical [3], or vibration energy sources [4]. For systems that can only access very weak energy sources (e.g., nW/mm$^2$ power density [5]), micro-batteries can be used for energy storage to sustain the system operations [6], [7]. Therefore, the power budget of most self-powered systems is several microwatts to a few 10's of microwatts in order to maintain the system sensitivity or the micro-battery efficiency. For example, the system power of [2] and [3] are 10 $\mu$W and 6 $\mu$W, respectively; and the standard discharge power of the micro-battery SR512SW is only 8 $\mu$W [7]. Therefore, power consumption of the embedded sensor must be of sub-microwatt to meet this system constraint. In addition, peak current of the embedded sensor must be minimized to avoid system level failure as a result of the sudden supply collapse, especially for energy harvester-powered systems with small storage capacitors [2]. For systems supplied by micro-batteries, the large source resistance of the micro-battery (e.g., 7∼60 kΩ [6]) even mandates a sub-microampere peak current of the sensor to minimize the supply fluctuation, which is a challenge for many low-power sensors, like [8].

For temperature sensor design in self-powered systems, instead of using delta-sigma data converters [8], duty cycle or frequency modulation schemes are favored as they do not need decimation filters and can better reuse the system resources such as clock and digital baseband for power saving [1]. Using such time-domain schemes has enabled many sensor designs with single digit $\mu$W power consumption [1], [2], [9]. However, as in [2], using typical comparators for duty cycle modulation imposes extra power to generate stable voltage references, which then degrades the sensor resolution figure of merits (R-FoM [10]), e.g., 1.5 nJ·K$^2$ [2]. This R-FoM was improved by using a Schmitt trigger for output modulation as evidenced in [11], which shows a superior 3.6 pJ·K$^2$ R-FoM but consumes 160 $\mu$W power. This power budget limits the applications of [11] in energy harvester- or micro-battery-powered systems. Therefore, a temperature sensor with low peak current and with power optimization in both its frontend and output modulation scheme is highly required.

In this brief, we present a temperature sensor frontend with device leakage and nonlinearity compensation, which reuses one regulation loop to generate both the proportional-to-absolute-temperature (PTAT) and complementary-to-absolute-temperature (CTAT) currents to achieve power saving. In addition, a current starved multivibrator is optimized for duty cycle modulation, which produces the required clamping voltages by reusing the current of the timing capacitor. As a result, the merits of simple interface and ratio-metric readout of [11] are maintained, while the sensor power is reduced to 0.9 $\mu$W and has only a sub-$\mu$A peak current. Meanwhile, compared with designs that use comparator or digital buffer for duty cycle modulation [1], [2], [9], higher energy efficiency is achieved (10.6 pJ·K$^2$). The rest of this brief is organized as follows. Section II describes the sensing concept. Section III details its CMOS implementations. Silicon results are shown in Section IV, followed by a conclusion in Section V.

## II. Sensing Concept

This sensor uses NPN bipolar junction transistor (BJT) as the sensing device for its temperature-sensitive base-emitter voltage [12]

$$V_{\rm be} = V_0 - \lambda T + C_{\rm nl} \tag{1}$$

where $V_0$ is the extrapolated $V_{\rm be}$ at 0 K; $\lambda$>0 is $V_{\rm be}$'s slope at a reference temperature $T_{\rm r}$, $C_{\rm nl} \propto (\eta - \zeta)\cdot{\rm Tln}({\rm T}/{\rm T_r})$ is the

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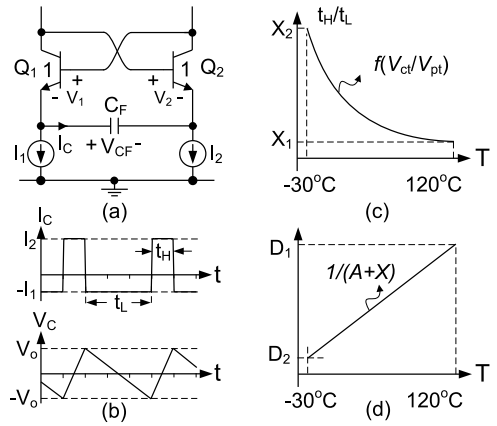


Fig. 1. (a) Basic multivibrator structure for duty cycle modulation; (b) terminal current and voltage of the timing capacitor $C_F$; (c) temperature dependency of $t_H/t_L$; (d) digital output of the sensor after linearize $X$.

nonlinear content in $V_{be}$, where $\eta \approx 3$ is a process parameter and $\zeta$ is the temperature exponent of the BJT's collector current. As a result, $V_{be}$ is CTAT. For two BJTs with different collector current densities, $\lambda$ varies and their $V_{be}$ difference $\Delta V_{be}$ is PTAT. $V_{be}$ ($V_{ct}$) together with $\Delta V_{be}$ ($V_{pt}$) are used for temperature sensing [8].

The simplified duty cycle modulation structure of this sensor is shown in Fig. 1(a). For this cross-coupling topology, only one of $Q_{1,2}$ is fully conducting at any particular instance. Hence, the timing capacitor $C_F$ is periodically charged up to $V_o$ by $I_2$ and discharged to $-V_o$ by $I_1$ [Fig. 1(b)]. For charge conservation, $I_1 \cdot t_L = I_2 \cdot t_H$ and $t_H/t_L = I_1/I_2 = X$. If $I_1 \propto V_{ct}$ and $I_2 \propto V_{pt}$, $X$ is a nonlinear function of temperature [Fig. 1(c)]. If $I_{ref} = I_1 + AI_2$ is temperature-independent, $I_2/I_{ref} = 1/(A+X)$ becomes linear, where $A$ is a design constant. Therefore, $X$ can be used for temperature sensing after linearizing it in the digital backend with 1/(A+X) [Fig. 1(d)]. Similar to [11], $X$ relies on the ratio of $I_{1,2}$. $V_o$ variation caused by the spread or mismatch of $Q_{1,2}$ can only affect $I_{1,2}$ via the current mirrors, which can be designed negligible by high impedance implementations.

Ideally, in Fig. 1(a), the transition from one quasi-stable state to another happens when $V_1$ ($V_2$) is higher than the turn-on voltage of $Q_1$ ($Q_2$). Such an inherent transition threshold avoids the use of comparator with clean voltage reference, resulting in higher energy efficiency than [1], [2], [9].

## III. CMOS Implementation

### A. Sensing Frontend and Nonidealities

The proposed sensing frontend is shown in Fig. 2, which generates a PT current $I'_{pt}$, a CT current $I'_{ct}$, and a BJT base current replica $I_b$. All these currents are copied by self-cascode PMOS or low voltage cascode NMOS current mirrors for further processing. In Fig. 2, $Q_{2,3}$ have the same collector bias current and an emitter area ratio of $p$. Meanwhile, $Q_{2,3}$, the self-cascode transistors $M_{p5\text{-}8}$ and a tail resistor $R_{ss}$ form a high gain amplifier $A_0$. As a result, the feedback loop via $M_{p3,4}$ and $A_0$ develops a PTAT voltage $\Delta V_{be} = V_T \cdot ln(p)$ across $R_{pt}$, where $V_T$ is the thermal voltage. This regulation loop is stabilized by $C_c$ and $R_z$. After matching (to the first-order) $Q_{2,3}$'s base resistances with a 180 Ω p-plus resistor $R_b$ and matching their collector to substrate leakage with $Q'_{2,3}$, $\Delta V_{be}$ becomes highly linear (~3.5 °C error at 120 °C if without $Q'_{2,3}$). In Fig. 2, $M_{p17,18}$, $M_{n1,2}$ and $M_0$ (high-$V_T$ for small off-state leakage) form a start-up circuit. After power-on, $M_0$ gradually charges up the base nodes of $Q_{2,3}$ and turns them on. Once $I'_{ct}$ is large enough, $V_{st}$ developed by $M_{n1,2}$ gradually turns $M_0$ off and the circuit enters into its normal operation.

A Darlington pair $Q_{0,1}$ is added to the output stage of the error amplifier to develop a CTAT voltage over $R_{ss}$, and

$$V_{Rss} = V_{be0} + V_{be1} - V_{be2} - R_b I_{b2}. \tag{2}$$

In Fig. 2, the CTAT current $I_{ss}$ developed by $R_{ss}$ is reused as the tail current of $A_0$ for power-saving. By ignoring the influence of $R_b$ and assuming the forward current gain $\beta_F$ of $Q_{2,3}$ are the same, $I'_{pt}$ and $I'_{ct}$ in Fig. 2 are

$$I'_{pt} = \frac{\Delta V_{be}}{R_{pt}} + I_{b3}, \tag{3}$$

$$I'_{ct} = \frac{V_{Rss}}{2R_{ss}} - I_{b3}. \tag{4}$$

Both $I'_{pt,ct}$ contain a copy of $Q_3$'s base current $I_{b3}$ and their linearities are degraded because $\beta_F(T_r)$ of $Q_{2,3}$ (75 nA nominal bias) is only 10~15. To linearize $I'_{pt,ct}$, a $I_{b3}$ replica ($I_b$ in Fig. 2) is produced by $M_{p9\text{-}12}$, $Q_4$, $2R_{ss}$ and an error amplifier $A_1$, where $A_1$ is a current-mirror-loaded NMOS differential pairs with a tail current of 15 nA. Due to the high impedance of $M_{p7\text{-}10}$, a 20 mV voltage difference between node A and C only causes ~3 pA current difference between $M_{p7,8}$ and $M_{p9,10}$. This means $A_1$ with a moderate gain (designed to be 42 dB) and a relaxed input offset suffices.

In (4), besides $I_{b3}$, $I'_{ct}$ is also affected by the curvatures $C_{nl0\text{-}2}$ (concave shape) in $V_{be0\text{-}2}$. In this design, the collector current of $Q_0$ is $\beta_F/(1+\beta_F) \cdot I_{pt} \approx I_{pt} \propto T$. Therefore, $\zeta_0 \approx 1$ and $C_{nl0} \approx 3.5$ mV, which is comparable to a typical PTAT-biased BJT [13]. For $Q_2$, its collector current is CTAT, and the resulting $C_{nl2}$ can be as large as 8 mV. In order to linearize $V_{Rss}$ in (2), $C_{nl1} \approx C_{nl2}\text{-}C_{nl0}$ should hold. For $Q_1$, its overall collector and base current is ~5 nA (base current of $Q_0$). For BJT with such a small bias current, its $\beta_F$'s nominal value and temperature exponent vary with its collector current density, which further affects its $V_{be}$ linearity [12]. In Fig. 2, the collector current of $Q_1$ is $\beta_F/(\beta_F+1)^2 \cdot I_{pt}$, which is highly $\beta_F$-dependent. During design, n=16 is selected for $Q_1$ to adjust $\beta_F$ to linearize $V_{Rss}$, and the simulated $C_{nl1} \approx 5$ mV.

Table I shows the critical device sizes and coefficients of this sensing frontend. The simulated $I'_{pt,ct}$ and $I_b$ are shown in Fig. 3(a). To utilize the output dynamic range, $X = I_1/I_2$ is designed to be 5.3 and 0.1 at -30 °C and 120 °C, respectively; which is achieved by the linear combination of $I'_{pt,ct}$ and $I_b$, with $I_1 = I'_{ct} + I_b - 1/2 I'_{pt}$ and $I_2 = I'_{pt} - 3/2 I_b - 2/5 I'_{ct}$, as shown in Fig. 3(b). The coefficients are selected to achieve high-order compensation after linearizing $X$. As shown in Fig. 3(c), a maximum -0.45/+0.3 °C nonlinear error remains in the frontend at different corners. Because $X$ is process-dependent [8], trimming is needed to minimize the inter-die variations (discussed in Section III-C).

### B. Duty-Cycle-Modulated Output

The current-starved multivibrator is shown in Fig. 4. BJTs are adopted to form the oscillator for their higher transconductances compared with MOSFETs. At start-up, assuming $Q_0$ is on and $Q_1$ is off, the node voltage

$$V_1 = V_L = V_{DD} - R_0 \frac{\beta_F}{1+\beta_F}(I_1 + I_2), \tag{5}$$

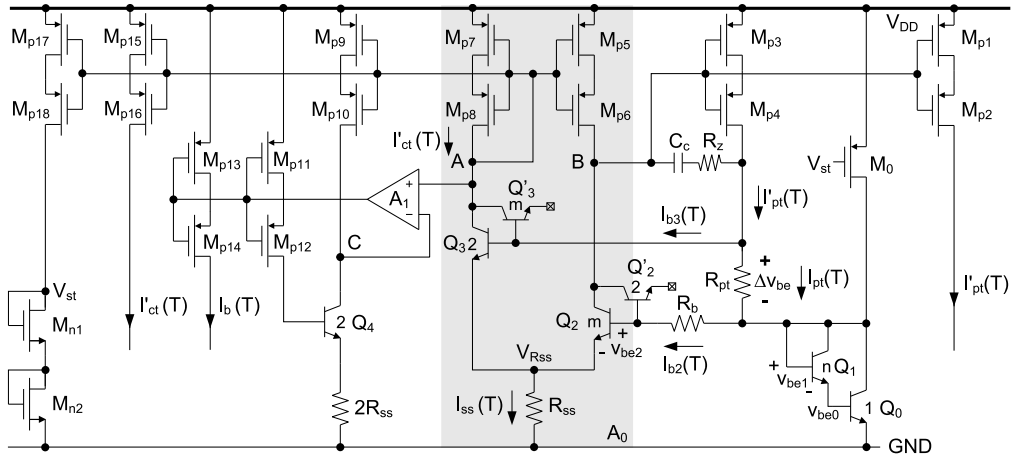


Fig. 2. Simplified self-regulated temperature sensor frontend with BJT base current replica for nonlinearity compensation (output current mirrors not shown).

TABLE I
CRITICAL DEVICE SIZES AND COEFFICIENTS

| | | | |
|---|---|---|---|
| $M_{p3}$ W/L($\mu$m) | 0.36/10.8×6 | $M_{p4}$ W/L($\mu$m) | 2.36/1.08×6 |
| $M_{p5,7}$ W/L($\mu$m) | 0.36/10.8×5 | $M_{p6,8}$ W/L($\mu$m) | 2.36/1.08×5 |
| $R_{pt}$, $R_{ss}$ (p+ poly) | 538K, 3.23M | $m$, $n$ | 8, 16 |

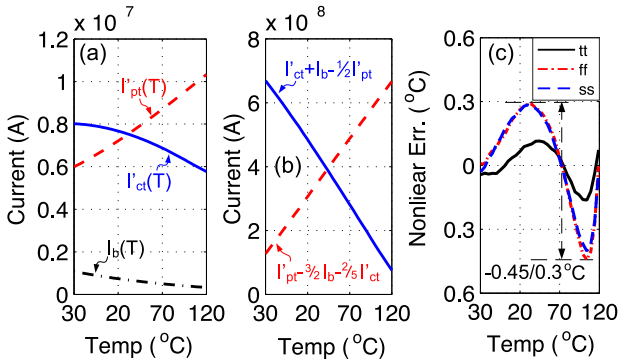


Fig. 3. (a) Currents over temperature; (b) combination of $I'_{pt,ct}$, $I_b$ for nonlinear compensation and a maximized dynamic range; (c) frontend nonlinearity error.

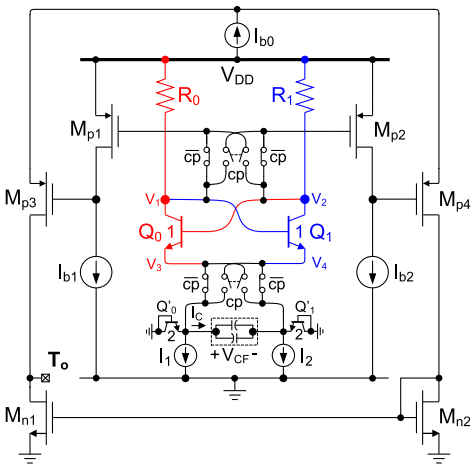


Fig. 4. Simplified multivibrator for duty cycle modulation ($I_{b0}$=30 nA, $I_{b1,2}$=11.5 nA, $R_0$=$R_1$=4.3 MΩ, MIM capacitor $C_F$=16 pF).

$$V_2 = V_H = V_{DD} - R_1 \frac{1}{1+\beta_F}(I_1 + I_2), \tag{6}$$

where $R_0$=$R_1$. After amplifying $V_{1,2}$ by $M_{p1,2}$, followed by a rail-to-rail buffer formed by $M_{p3,4}$, $M_{n1,2}$, the logic of $T_o$ is 'high'. At the same time, $V_3$ is kept constant at $V_H - V_{be}$ and $V_4$ gradually decreases because $C_F$ is discharging by $I_2$. Once $V_4$=$V_L$-$\alpha V_{be}$, the circuit state changes: $Q_0$ turns off, $Q_1$ turns on and $T_o$ becomes 'low'. Due to the subthreshold conduction of BJT, the turn-on voltage of $Q_{0,1}$ is $\alpha V_{be}$ instead of $V_{be}$, where $0< \alpha <1$ and varies with temperature. The node voltages $V_{3,4}$ become $V_H$-$V_{be}$ and $2V_H$-$V_L$-$(2-\alpha)V_{be}$, respectively. As a result, the voltage swing of $C_F$ is

$$V_{FS} = 2[V_H - V_L + (\alpha - 1)V_{be}] \tag{7}$$

Since both charging and discharging of $C_F$ are referenced to $V_{FS}$, $\alpha$ does not affect the duty cycle of $T_o$. Moreover, in (7), $V_{FS}$ only has a weak dependency on $V_{DD}$. This characteristic is essential for systems that do not have the power budget to afford LDOs with strong supply and load transient regulation (e.g., [1] and [2]). In Fig. 4, for minimal kickback noise, $M_{p1,2}$ isolate $V_{1,2}$ from the output that has large voltage swing. Fig. 5 shows the simulated waveforms of $V_{1,3,4,CF}$, $T_o$ and $Q_{0,1}$' on-off states. The overall peak current of this sensor is below 50 nA (except during start-up) as all current branches are starved.

To minimize the sensing error, $C_F$ consists of two end-to-end connected capacitors to match the node capacitances of $V_{3,4}$ (Fig. 4). Secondly, to mitigate the device mismatch induced unbalanced state transition time of the multivibrator, every temperature reading consists of different outputs with the control signal cp=0 or 1 to change the roles of $R_{0,1}$ and $Q_{0,1}$. Thirdly, to compensate the off-state leakages of $Q_{0,1}$ (causes ±0.1 °C error at the two temperature ends), BJTs $Q'_{0,1}$ with 2× area are included to effectively cancel >75% of such leakage effect. Finally, the multivibrator's switching time $t_s$ (5, 4 $\mu$s at -30, 120 °C, respectively) depends on its tail current $I_{1,2}$ and temperature [14]. Its output pulse width $t_L$+$t_H$ is therefore designed much longer (e.g., 270 $\mu$s at 30 °C) than $t_s$ by using a large 16 pF $C_F$. This can keep $t_s$ induced nonlinear error below ±0.05 °C at the cost of an increased chip area.

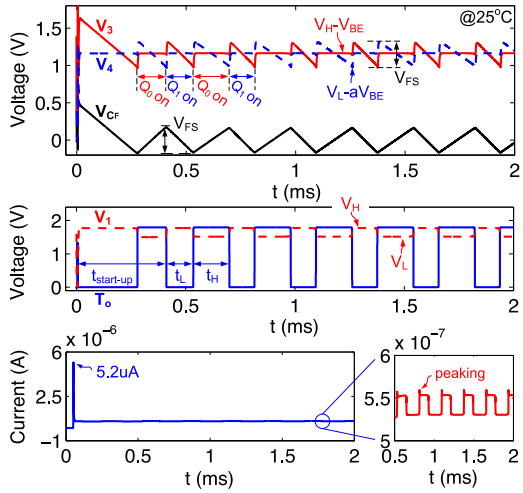


Fig. 5. Waveforms of $V_{3,4}$, $V_{CF}$ (top) and $V_1$, $T_o$ (middle) of Fig. 4; instantaneous sensor current during start-up and normal operation (bottom).

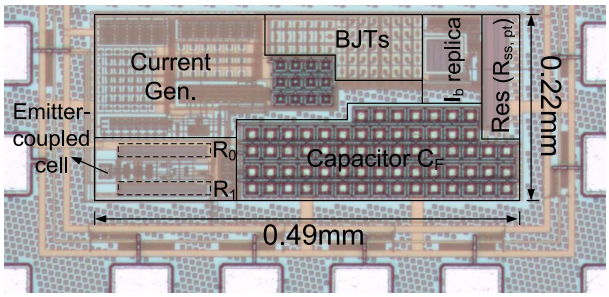


Fig. 6. Chip micrograph of the sensor.

### C. Trimming

In this design, any error in $I_{1,2}$ can degrade the sensing accuracy. Among the error sources, resistor spreads do not affect $X$ for its ratiometric property. Saturation current spreads of $Q_{0\text{-}2}$ however introduces a PTAT spread into $I'_{ct}$. In this design, CTAT and PTAT signals are linearly combined to form $I_{1,2}$. As a result, both $I_{1,2}$ have PTAT spreads, which introduces a gain and an offset error into $X$. This error can be trimmed by

$$D_o|_{trimmed} = \frac{1}{A + \dfrac{X_{out} - \gamma/\alpha}{1-\gamma}}, \tag{8}$$

where $A$ is the nominal design constant discussed in Section II. $\alpha$=-2/5 is the coefficient of $I'_{ct}$ in $I_2$. The trimming factor $\gamma$ in (8) can be calculated by comparing the actual output $X_{out}$ with the target output $X_{ideal}$ at the trimming temperature $T_r$,

$$\gamma = \frac{X_{ideal}|_{Tr} - X_{out}|_{Tr}}{X_{ideal}|_{Tr} - 1/\alpha}. \tag{9}$$

Other PTAT spreads in $I_{1,2}$ caused by device mismatches can also be trimmed by (8). Overall, the cost of this thermal calibration process is comparable to that of [11], and data from one temperature point is needed. Ideally, the sensor error profile after trim should look like that of Fig. 3(c) with the curve been slightly rotated around $T_r$ for different sensors. However, $\beta_{F0\text{-}2}$ spreads introduce a nonlinear $\delta_{\beta_F}/[(1+\beta_F)R_{ss}]$ current into $I'_{ct}$, which can increase the output nonlinearity. More importantly, without DEM, $\beta_F$ mismatch of $Q_{3,4}$ and current mismatch of $M_{p7\text{-}10}$ may cause a big difference between $I_b$ and $I_{b3}$. Such a difference results in over- or under-compensation of $I_{b3}$ for $I'_{pt,ct}$, which changes the effective high-order compensation. In this case, the sensor precision after trimming would be limited by its linearity instead of the inter-die spread. The final sensor error profile can also deviate from the designed case as in Fig. 3(c).

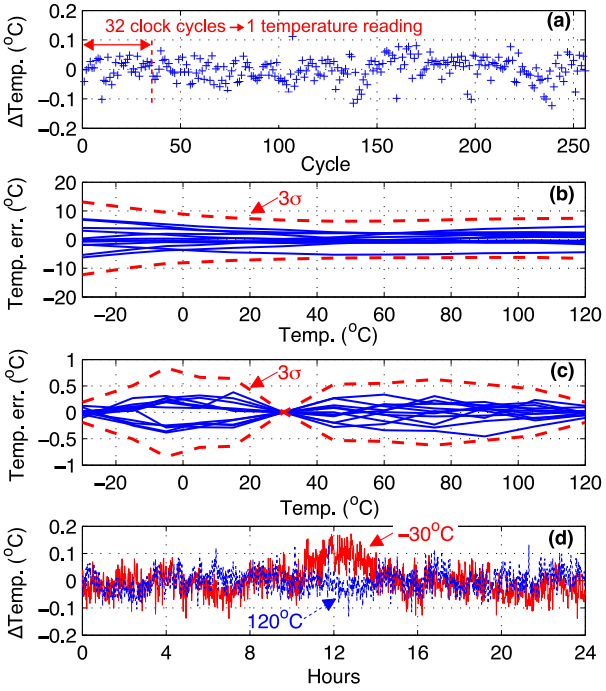


Fig. 7. (a) Output clock cycle-to-cycle variation at 30°C; (b) sensing inaccuracy without trim (12 samples); (c) sensing inaccuracy after an ideal individual trim at 30°C; (d) long-term operation of the sensor at extreme temperatures.

## IV. Measurement Results

The sensor prototype fabricated in a standard 0.18 $\mu$m CMOS process occupies 0.1 mm$^2$ area (Fig. 6). Measurements were performed from -30 °C to 120 °C in a climate chamber, where the prototype and a calibrated PT-100 sensor are placed in a metal thermal filter. Data acquisition is carried out with Opal Kelly XEM3001 board and its internal 48 MHz clock (0.25 ns peak-to-peak period jitter) is used for period counting.

The sensor draws 0.54 $\mu$A from a 1.6 V supply at 30 °C, with its maximum peak current measures below 50 nA. Fig. 7(a) shows the exemplary cycle-to-cycle variation of the output $T_o$ from the multivibrator (Fig. 4). To improve the sensor resolution, 32 consecutive cycles are averaged to form one temperature reading, corresponding to a kT/C-limited resolution of 39 mK (standard deviation after averaging 32 cycles). As one temperature reading takes 8.1 ms, the sensor resolution FoM is 10.6 pJ·K$^2$. To characterize the inter-die spread, outputs from 12 dies are compared against the reference sensor. After linearization, the sensing error without trimming is as large as 8 °C at -30 °C [Fig. 7(b)]. A single-point trimming at 30 °C reduces the spread to ±0.85 °C (3$\sigma$) [Fig. 7(c)]. The sensor was also tested at extreme temperatures for 24 hours, Fig. 7(d) shows its excellent stability (the static temperature change is due to the chamber dynamics). The longest start-up

TABLE II
COMPARISON WITH RECENTLY REPORTED STATE-OF-THE-ART TEMPERATURE SENSORS

| | [1][1] JSSC 10 | [2][1] TCAS-I 14 | [8] JSSC 13 | [11][1] ISSCC 14 | [13] JSSC 17 | [15] VLSIC 16 | **This Work[1]** |
|---|---|---|---|---|---|---|---|
| Technology ($\mu$m) | 0.18 | 0.18 | 0.16 | 0.7 | 0.16 | 0.028 | 0.18 |
| Active area (mm$^2$) | 1.1[2] | 0.14 | 0.08 | 0.8 | 0.16 | 0.0038 | 0.1 |
| Supply (V) | 1 | 1 & 1.35[3] | 1.5 to 2 | 2.9 to 5.5 | 1.5 to 2 | 1.1 to 2 | 1.6 to 2.0 |
| Nominal current ($\mu$A)* | 0.9 | 0.35 & 0.6 | 3.4 | 55 | 4.6 | 16 | **0.54** |
| Temp. range (°C) | -20 to 30 | -30 to 60 | -55 to 125 | -45 to 130 | -55 to 125 | -20 to 130 | -30 to 120 |
| DC supply sensitivity (°C/V) | N/A | N/A | 0.5 | 0.05 | 0.01 | 0.012 | 0.7 |
| Sensing inacccuracy (°C) | ±0.8 (1-point) | ±1.5 (1-point) | ±0.15 (1-point) | ±0.15 (1-point) | ±0.06 (1-point) | ±1.8 (1-point) | ±0.85 (1-point) |
| Rel. IA (%) | 3.2 | 3.3 | 0.2 | 0.2 | 0.07 | 2.4 | 1.1 |
| Resolution (m°C) | 350 | 300 | 20 | 3 | 15 | 500 | 39 |
| Measurement time (ms) | 40 | 14.5 | 5.3 | 2.2 | 5 | 0.03 | 8.1 |
| Resolution FoM (pJ · K$^2$) [10] | 4.4×10$^3$ | 1.5×10$^3$ | 10.8 | 3.2 | 7.8 | 140.8 | **10.6** |

*Do not include clock and digital backend power; [1]Duty cycle-/frequency-modulated output; [2]Whole system; [3]1 V for readout and 1.35 V for front-end.

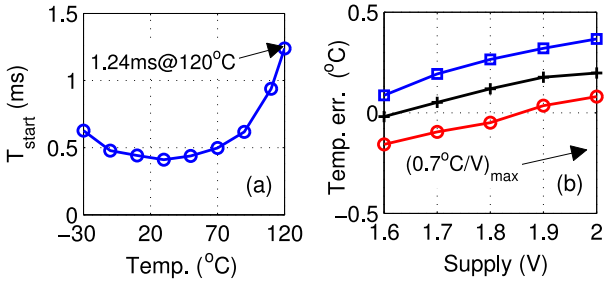


Fig. 8. (a) Measured startup (stabilization) time of the sensor at different temperatures; (b) supply sensitivity of 3 samples at 120 °C.

time of the sensor is 1.24 ms at 120 °C [Fig. 8 (a)]. Meanwhile, due to the self-regulation and the use of self-cascode transistors, the measured worst case supply sensitivity is 0.7 °C/V over a supply voltage from 1.6 to 2 V [Fig. 8(b)].

The sensor performance is summarized in Table II and benchmarked with the state-of-the-art BJT-based sensors with microwatt to sub-microwatt power. In this brief, the focus is to design a sub-microwatt sensor with simple interface, small peak current and reasonable energy efficiency that can be used in self-powered systems. For R-FoM defined as Energy/Conversion×Resolution$^2$ in [10], this sensor is among the state-of-the-art (except [11]) while consumes the least power. For wireless sensing platform, precision of this sensor is reasonable and still has room to be improved by adopting more dynamic error correction techniques.

## V. CONCLUSION

We have presented a duty-cycle-modulated temperature sensor with a sub-$\mu$W power, a sub-$\mu$A peak current and a simple sensor interface. Different from conventional sensing frontends, a compact one is proposed to achieve low-power operation, along with device-level leakage and linearity compensation techniques used to maintain a reasonable precision. In addition, multivibrator with inherent clamping threshold is optimized for duty cycle modulation, leading to a higher R-FoM (10.6 pJ·K$^2$) as opposed to the comparator with voltage reference schemes. The designed temperature sensor can be applied in both power- and energy-limited systems.

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